Circuit Transformer: A Transformer That Preserves Logical Equivalence

Xihan Li[1], Xing Li[2], Lei Chen[2], Xing Zhang[2], Mingxuan Yuan[2], Jun Wang[1]
[1] University College London [2] Huawei Noah's Ark Lab, Hong Kong
{xihan.li,jun.wang}@cs.ucl.ac.uk
{li.xing2,lc.leichen,zhangxing85,Yuan.Mingxuan}@huawei.com

Abstract

Despite the significant advancements in next token prediction models, they are often considered less promising for logic tasks that demand exact precision. In this study, we introduce an end-to-end Transformer model, the "Circuit Transformer", which ensures such exactness by generating new logic circuits that are strictly equivalent to existing ones. This is accomplished through a novel approach that formulates equivalent circuit generation as a constrained sequential generation process for backtrack programming. Then we propose a top-down and sequential circuit representation method with advantageous "cutoff properties", enabling next-token prediction models to generate circuits in a manner similar to natural language generation, while strictly adhering to the feasible region. This equivalence-preserving property also allows optimization methods to explore freely without violating constraints. Experimentally, we trained an 88-million-parameter Circuit Transformer to generate equivalent yet more compact forms of input circuits, outperforming existing neural approaches on both synthetic and real world benchmarks, without any violation of complex equivalence constraints.

1 Introduction

In this work, we focus on generating a proper logic gate implementation g of a Boolean function

$$\boldsymbol{y} = f(\boldsymbol{x}), \tag{1}$$

in which $\boldsymbol{x} = (x_1, \dots, x_N) \in \{0,1\}^N$ is the N-dimensional input, $\boldsymbol{y} = (y_1, \dots, y_M) \in \{0,1\}^M$ is the M-dimensional output. While a Boolean function f may have many different logic gate implementations g, all these implementations are strictly constrained by the logical equivalence. That is defined as $g \in C(f)$, in which

$$C(f) = \{g | g_i(\boldsymbol{x}) = f_i(\boldsymbol{x}) \quad \forall \boldsymbol{x} \in \{0,1\}^N, i = 1, \dots, M\} \tag{2}$$

is the feasible region of g under f consisting of $2^N \cdot M$ equality constraints. A logic gate implementation g of a Boolean function is also called a *circuit*. [1] An example is shown in Figure 1.

This equivalent circuit generation problem is highly concerned in the fields of Boolean algebra and computational complexity theory, especially in the context of finding a compact form of a circuit g with minimal number of logic gates (circuit size minimization). That is

$$\mathbf{min}\, |g'| \quad \mathbf{s.t.} \quad g' \in C(g), \tag{3}$$

where $|g'|$ is the number of logic gates[2] in g'. This leads to important research areas such as logic optimization [43], minimum circuit size problem [14, 11] and circuit complexity theory [42, 35].

[1] More specifically, combinatorial logic circuit, which is referred to as "circuit" in short in this paper unless otherwise stated.

[2] NOT gates (inverters) are not counted in our paper to align with the mainstream research setting.

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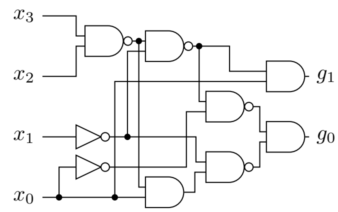
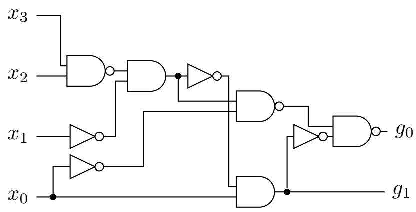
x_3	x_2	x_1	x_0	y_1	y_0	x_3	x_2	x_1	x_0	y_1	y_0
0	0	0	0	0	1	1	0	0	0	0	1
0	0	0	1	0	0	1	0	0	1	0	0
0	0	1	0	0	0	1	0	1	0	0	0
0	0	1	1	1	1	1	0	1	1	1	1
0	1	0	0	0	1	1	1	0	0	0	0
0	1	0	1	0	0	1	1	0	1	1	1
0	1	1	0	0	0	1	1	1	0	0	0
0	1	1	1	1	1	1	1	1	1	1	1

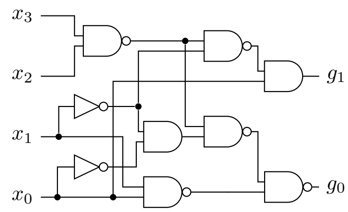
(a) A Boolean function $(y_1, y_0) = f(x_3, x_2, x_1, x_0)$, in which $x_0, x_1, x_2, x_3, y_0, y_1 \in \{0, 1\}$.



(b) An initial feasible implementation of the Boolean function f in Figure 1a, with 7 AND/NAND gates.



(c) A feasible implementation of f with 5 AND/NAND gates, which is optimal in size.



(d) An infeasible implementation. In this circuit $g_0 = 0 \neq y_0$ when $\boldsymbol{x} = (1, 1, 0, 1)$.

Figure 1: An example showing how a Boolean function can be implemented by circuits, i.e., cascade connections of logic gates. and are the AND gate and NOT gate respectively, and is the NAND gate, an AND gate followed by a NOT gate. The circuits shown in Figure 1b and Figure 1c are both *feasible* implementations of f, while the latter is more compact in size. The circuit shown in Figure 1d is *infeasible*, even if the difference is as small as one bit out of 32.

Practically, it also lies in the core of electronic design automation (EDA) in the semiconductor industry, as chips are built upon basic logic gates to fulfill certain Boolean functionalities. A compact circuit allows for more chips to be fabricated on a wafer, or more components to be integrated in a single chip, thereby heavily impacting the cost and performance of final chip products.

However, like many other logical and constrained tasks, symbolic approaches have taken the lead of tackling the aforementioned problem for decades, both in theory and practice. For the circuit size minimization problem, it is typically reduced to a series of Boolean satisfactory (SAT) problems and then solved via SAT solvers [17, 15, 37, 10]. More scalable methods in the EDA industry involve multiple heuristic operators, which are executed sequentially in a pre-defined operator sequence to reduce the size of an initial implementation [3, 23, 53]. While machine learning (ML) approaches emerge in recent years, they tackle sub-problems in aforementioned methods, such as SAT solver acceleration [32, 44, 51, 9] and operator sequence scheduling [48, 12, 8, 52, 46]. Direct generation of feasible circuits in the context of ML is regarded as extremely difficult, due to the complicated constraints and strict feasibility requirement [13, 21, 38, 29].

In this work, we firstly drive next token prediction models — especially Transformer models — to generate strictly feasible circuits while preserving logical equivalence. We model the problem of equivalent circuit generation as a constrained sequential pattern generation process, which can be solved with backtrack programming, a promising framework for constraint satisfaction. Then, we proposed a sequential representation of circuits, with associated "cutoff properties" so as to cooperate with backtrack programming. With top-down specification, three-valued logic and short-circuit evaluation techniques introduced, our proposed cut-off properties for backtrack programming owns beneficial characteristics, allowing smooth inference of circuits analogous to typical natural language generation, while the equivalence constraints are strictly satisfied. With tree-based positional encodings [33], such a representation can also serve as a decent neural encoding of circuits. Finally, a transition approach is proposed to enable tree-based generation method to generate directed acyclic graphs via merging nodes with equivalent functionalities.

Moreover, such an equivalence-preserving representation enables decisional optimization methods to efficiently generate equivalent circuit with desired objective (e.g., size minimization). Without the barrier of constraint violation, equivalent circuit generation can be modelled as a Markov decision process with a fixed action space. The only requirement is to designate an immediate reward function to reflect the optimization goal. An example on circuit size minimization problem is also attached.

To demonstrate the effectiveness of our proposed techniques, we developed an end-to-end approach to tackle the aforementioned circuit size minimization problem. A Transformer model of 88 million

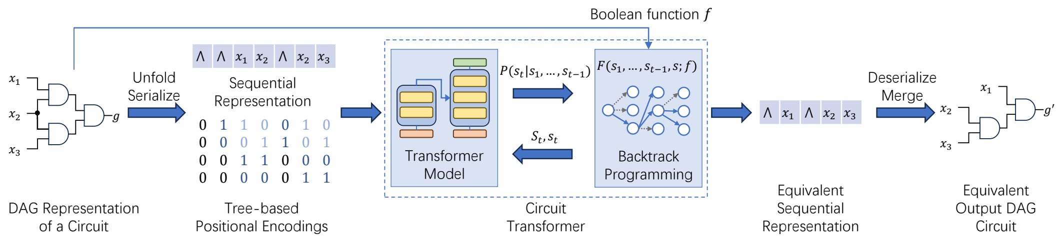


Figure 2: The pipeline of Circuit Transformer that transforms a circuit to a strictly equivalent one. The backtracking programming module acts as a masking layer at the end of the Transformer decoder.

parameters is trained in a supervised way to generate strictly equivalent yet more compact implementations of given circuits. Experimental results show that the trained model is capable of generating strictly equivalent implementations for *all* unseen circuits in the test set, and the size decrease is close to the traditional method that serves as the supervised signal.

To conclude, we make the following contributions:

- A novel formulation of the equivalent circuit generation problem as a sequential pattern generation process for backtrack programming.
- A sequential circuit representation method with beneficial cutoff properties, that allows next token prediction models to generate strictly equivalence-preserving circuits analogous to natural language generation, and can also serve as a neural encoding of circuits.
- A formulation of circuit optimization as a Markov decision process, with an immediate reward function assigned to reflect the optimization goal.
- An end-to-end Transformer model "Circuit Transformer" that allows transformation between logic circuits with strict equivalence preserved, with extensive experiments on the circuit size minimization problem demonstrating its exact feasibility of complex equivalence constraints.

2 Related Work

Recent years have witnessed the tremendous success of next token prediction models, especially Transformer models [41] behind mainstream large language models (LLM). However, due to their probabilistic nature, such models are usually less promising in domains requiring exact preciseness. Therefore, the mainstream paradigm of ML in such domains is to aid traditional methods in solving sub-problems that are more relaxed with respect to exactness. For example, AlphaGeometry [40] trained a Transformer model to aid geometry theorem proving, which requires strict exactness, by suggesting candidate auxiliary points that does not require such exactness. In the context of circuit design, such relaxed sub-problems include SAT solver acceleration [32, 44, 51, 9], circuit representation learning [50, 47, 19, 45], learning based graph optimization [28, 20], operator sequence scheduling [48, 12, 8, 52, 46], and placement and routing [22, 5].

Nonetheless, there are a few research works [31, 30, 6] that attempt to generate circuits or logical expressions directly via next token prediction models. However, none of them takes feasibility guarantee into consideration, and not surprisingly, failure cases do commonly exist in their reported results, which limit their practical usage. In [31], 20% - 70% generated circuits violate the input specification in different datasets, while a follow-up work [30] mitigates the invalid percentage to 16% - 65% with pre-trained language models. In [6], 5% - 10% cases failed to be fully recovered when the number of operators are between 25 and 50. Apart from the low-level circuit generation, many researchers focus on transferring the software code generation capability of LLM to high-level hardware code generation, but these methods still suffer from functional inequivalence [21, 38, 29].

There are also research works that guarantee the feasibility of solutions via action masking, especially for problems involving routing such as maze game, traveling salesman problem, and vehicle routing problem [27, 18, 7]. However, these problems are usually intuitive to be sequentially modelled, allowing action masks to simply filter invalid actions such as wall-hitting directions and visited cities. Action masking techniques under complicated constraints have yet to be explored.

For sequential representation of gate-level circuits, existing formats include graph-based ones like AIGER [2] and BLIF [1], and code-based ones like Verilog [39] and VHDL [36]. The former ones specify a logic circuit by listing all the gates with their connection to child nodes, which can be regarded as a specialization of adjacency list to represent a graph. The latter ones are more general hardware description languages that are close to programming languages in format. However, they lack essential characteristics that allow cutoff properties to be defined under the framework of backtrack programming.

3 Methods

To ensure that next-token prediction models consistently produce circuits that meet all $2^N \cdot M$ equivalence constraints specified in Equation 2, we integrate these models with a backtracking programming framework. We then introduce a novel sequential representation of circuits designed to work efficiently within this framework. Additionally, we propose a Markov decision process formulation to optimize the generated circuits while maintaining equivalence.

3.1 Equivalent Circuit Generation with Backtrack Programming

Next token prediction targets *sequential generation*, that is, a series of tokens $s_1, s_2, \ldots$ is sampled from a probability distribution $P(s_t|s_1, \ldots, s_{t-1})$ in a recursive manner. To generate sequences $s_1, \ldots, s_n$ with strict constraints to make sure that certain property $F(s_1, \ldots, s_n) \in \{0, 1\}$ holds, a promising approach is backtrack programming [16]. It involves the invention of intermediate "cutoff" properties $F(s_1, \ldots, s_t)$ for $1 \leq t < n$, which have the following two characteristics

Characteristic 3.1 (Inheritability). *$F(s_1, \ldots, s_t)$ is true whenever $F(s_1, \ldots, s_{t+1})$ is true;*

Characteristic 3.2 (Incrementality). *$F(s_1, \ldots, s_t)$ is fairly easy to test, if $F(s_1, \ldots, s_{t-1})$ holds.*

Proper cutoff properties allow candidate sequences to be incrementally built towards the solution, and backtrack when a candidate cannot possibly be completed to a feasible solution. Given partial sequence $s_1, \ldots, s_t$ at time step t that $F(s_1, \ldots, s_t)$ holds, the feasibility of the next token s_{t+1} can be tested quickly via $F(s_1, \ldots, s_t, s_{t+1})$, and backtrack can occur when all s_{t+1} has been recursively explored. A detailed introduction of the framework is leaved in the appendix.

Following this direction, to leverage next token prediction to generate strictly equivalent circuits, we aim to find a proper sequential representation of circuits, as well as proper cutoff properties in each step to indicate the equivalence, so that we can remodel the equivalent circuit generation problem

$$\textbf{find} \quad g \quad \textbf{s.t.} \quad g \in C(f) \tag{4}$$

as a constrained generation process of sequential patterns

$$\begin{aligned} \textbf{find} \quad & s_1, s_2, \ldots, s_n \\ \textbf{s.t.} \quad & F(s_1, \ldots, s_t; f) \text{ holds}, t = 1, \ldots, n \\ & s_1, \ldots, s_n \text{ represents a unique circuit} \end{aligned} \tag{5}$$

so as to apply backtrack programming to guarantee the feasibility. In Equation 5, $s_1, \ldots, s_t$ is a series of sequential patterns and represents a class of circuits, which will be elaborated in the next section. $F(s_1, \ldots, s_t; f)$ is the cutoff property in step t, which holds if and only if the circuits represented by $s_1, \ldots, s_t$ are all within the feasible region $C(f)$.

In such a way, given a next token prediction model

$$P(s_t|s_1, \ldots, s_{t-1}) \tag{6}$$

that provides the probability distribution of s_t given the previous tokens $s_1, \ldots, s_{t-1}$, we can generate the circuit by Algorithm 1, which is an adaptation of the backtrack programming framework introduced in [16] with candidate tokens ordered by the probability distribution.

3.2 A Sequential Representation of Circuits with Cutoff Properties

With the new formulation in Equation 5 and Algorithm 1, the circuit generation problem reduces to finding a sequential representation $s_1, s_2, \ldots$ of circuits, with corresponding cutoff properties $F(s_1, \ldots, s_t; f), 1 \leq t < n$ satisfying Characteristic 3.1 and Characteristic 3.2 that keep the sequential representation within the equivalence class of f. Moreover, as our goal is to generate *one* rather than *all* feasible circuits, the most efficient circumstance in Algorithm 1 is that the "backtracking" process in line 11-14 is never executed. That is, $S_t \neq \emptyset$ all the time. Thus, it is desirable for an efficient representation to guarantee this, avoiding any compulsory backtracking when only a single circuit is required to be delivered. That is,

Algorithm 1 Equivalent Circuit generation with Backtrack Programming

Input: The Boolean function f that the generated circuit should be equivalent to. Next token prediction model $P(s_t|s_1, \ldots, s_{t-1})$.
Output: A feasible circuit g satisfying $g \in C(f)$.
1: $t \leftarrow 1$
2: **while** true **do**
3:     Compute a probability distribution of $s_t \in D$ by the next token prediction model

$$p_t \leftarrow P(s_t|s_1, \ldots, s_{t-1})$$

4:     Set $S_t \leftarrow \{s \in D|F(s_1, \ldots, s_{t-1}, s; f) \text{ holds}\}$
5:     **while** true **do**
6:         **if** $S_t \neq \emptyset$ **then**
7:             $s_t \leftarrow \arg\max_{s \in S_t} p_t(s)$
8:             **if** $s_1, \ldots, s_t$ represents a unique circuit **then return** the corresponding circuit
9:             $t \leftarrow t + 1$
10:             **break**
11:         **else**   ▷ The backtrack process. If Characteristic 3.3 holds, this branch will never be executed.
12:             $t \leftarrow t - 1$
13:             $S_t \leftarrow S_t \backslash s_t$
14:         **end if**
15:     **end while**
16: **end while**

a	**¬a**
1	0
0	1
U	*U*

(a) NOT operator

a ∧ b		**a**: **1**	**0**	**U**
b	**1**	1	0	*U*
	0	0	0	0
	U	*U*	0	*U*

(b) AND operator

a ∨ b		**a**: **1**	**0**	**U**
b	**1**	1	1	1
	0	1	0	*U*
	U	1	*U*	*U*

(c) OR operator

a ≃ b		**a**: **1**	**0**	**U**
b	**1**	1	0	1
	0	0	1	1
	U	1	1	1

(d) SIMEQ operator

Table 1: The truth tables for NOT, AND, OR and SIMEQ operators in three-valued logic.

Characteristic 3.3 (Backtrack Elimination)**.** *$S_t \neq \emptyset$ is always guaranteed in line 4 of Algorithm 1.*

In this way, the next-token prediction process can always proceed forward efficiently, analogous to typical natural language generation.

For tasks requiring exploration of feasible region for circuits, it is important for a representation of circuits to cover the widest possible (ideally all) feasible circuits, minimizing the miss of targets due to the restriction of representation. For example, while we can always generate a strict equivalent circuit for a Boolean function f via sum-of-product or product-of-sum forms, such forms are too restricted for any feasible region exploration. Therefore, we have the following desired characteristic:

Characteristic 3.4 (Completeness)**.** *For all $g \in C(f)$, there exists a sequence $s_1, \ldots, s_n$ that uniquely represents g.*

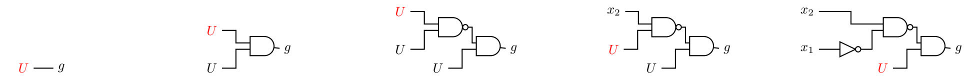
Now we propose a sequential representation of circuits with cutoff properties, that owns all the aforementioned characteristics.

First, while circuits are usually built in a bottom-up manner from inputs to outputs, we notice that the equivalence constraints are applied on each *output* of the circuit. That is, given the index of output i, a constraint $f_i(\boldsymbol{x}) = g_i(\boldsymbol{x}), \forall \boldsymbol{x} \in \{1, 0\}^N$ is only possible to be validated when the corresponding circuit output g_i has been built. Therefore, we adopt a special top-down order, specifying a circuit from outputs to inputs, to allow constraint validation throughout the construction process.

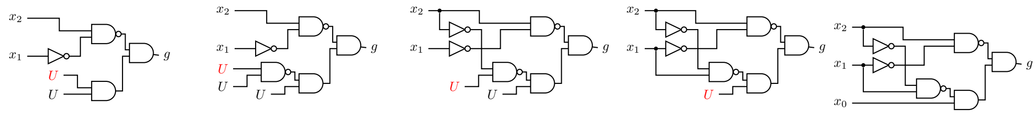
Then, to allow indeterminacy in the circuit representation, we include the three-valued logic into the circuit evaluation process. That is, besides $\{0, 1\}$ which indicate *false* and *true*, there is another truth value "U" which means *unknown*. The truth tables of such logic for NOT, AND and OR operators are shown in Table 1. Additionally, we define a binary operator "SIMEQ" ($\simeq$, is similar or equal to), which is equivalent to the equal operator ($=$) for $\{0, 1\}$, while accommodating U by $U \simeq 0$ and $U \simeq 1$. During the generation process, we relax the feasible region from Equation 2 to

$$C'(f) = \{g|g_i(\boldsymbol{x}) \simeq f_i(\boldsymbol{x}) \quad \forall \boldsymbol{x} \in \{0, 1\}^N, i = 1, \ldots, M\} \tag{7}$$

so that the occurrence of U in the output will not violate the constraint. For simplicity, here we assume $M = 1$ and leave multi-output cases to be discussed later. The generated circuit g is initialized to be



(a) The initial circuit. $S_0 = \{\wedge, \overline{\wedge}\}$, $s_0 = \wedge$.
(b) Step 1. $S_1 = \{x_0, \wedge, \overline{\wedge}\}$, $s_1 = \overline{\wedge}$.
(c) Step 2. $S_2 = D$, $s_2 = x_2$.
(d) Step 3. $S_3 = \{\overline{x_0}, \overline{x_1}, \overline{x_2}, \wedge, \overline{\wedge}\}$, $s_3 = \overline{x_1}$.
(e) Step 4. $S_4 = \{\wedge, \overline{\wedge}\}$, $s_4 = \wedge$.



(f) Step 5. $S_5 = \{x_0, \wedge, \overline{\wedge}\}$, $s_5 = \overline{\wedge}$.
(g) Step 6. $S_6 = D$, $s_6 = \overline{x_2}$.
(h) Step 7. $S_7 = \{\overline{x_0}, x_1, x_2, \wedge, \overline{\wedge}\}$, $s_7 = x_1$.
(i) Step 8. $S_8 = \{x_0, \wedge, \overline{\wedge}\}$, $s_8 = x_0$.
(j) The generated circuit.

Figure 3: An example showing how a strictly feasible circuit can be built with our proposed sequential representation with cutoff properties. $f(x_2, x_1, x_0)$ is a Boolean function with $f(0,1,0) = f(1,1,1) = 1$ and $f(x_2, x_1, x_0) = 0$ otherwise. $D = \{x_0, \overline{x_0}, x_1, \overline{x_1}, x_2, \overline{x_2}, \wedge, \overline{\wedge}\}$, U denotes the wildcard node, the next wildcard node to be replaced is marked in red. $S_t = \{s \in D | F(s_1, \ldots, s_{t-1}, s; f) \text{ holds}\}$.

a single constant node U, which we call "wildcard node" as it can potentially represent any feasible circuits. So initially, $g(\boldsymbol{x}) \equiv U$ no matter what the input $\boldsymbol{x}$ is. This is within the relaxed feasible region in Equation 7 but provides no information about the circuit structure.

Given the initial circuit, the sequential generation process acts as refining the circuit g by recursively replacing a wildcard node to a specific one $s_t \in D$, which can be either a new logic gate or a new primary input. For a new logic gate, all its inputs will be initialized to wildcard nodes that need further refinement. With the proposed top-down approach, the values of $g(\boldsymbol{x})$ for all $\boldsymbol{x} \in \{0,1\}^M$ in Equation 7 can always be evaluated throughout the construction process, following the truth tables in Table 1. Note that the introduction of three-valued logic also enables short-circuit evaluation with unknown values. For an AND gate $c(\boldsymbol{x}) = a(\boldsymbol{x}) \wedge b(\boldsymbol{x})$, if one of the inputs ($a(\boldsymbol{x})$ or $b(\boldsymbol{x})$) is evaluated to be 0 given specific $\boldsymbol{x}$, then $c(\boldsymbol{x}) = 0$ no matter what the other input is evaluated, even if it is U. The same logic applies for the OR gate when one of the inputs is evaluated to be 1.

Then, the cutoff properties $F(s_1, \ldots, s_t; f)$ holds if and only if for all $\boldsymbol{x} \in \{0,1\}^M$, the output of the constructed circuit $g^{(t)}$ given input $\boldsymbol{x}$ at time step t is similar or equal to $f(\boldsymbol{x})$. That is,

$$g^{(t)}(\boldsymbol{x}) \simeq f(\boldsymbol{x}), \quad \forall \boldsymbol{x} \in \{0,1\}^M \tag{8}$$

or simply, $g^{(t)} \in C'(f)$.

For the ending criteria, as a wildcard node can potentially be any circuit, only when all the wildcard nodes are recursively replaced by specific ones, can the sequence uniquely represent a circuit, which marks the end of the generation process in line 8 of Algorithm 1. For the order of replacement when multiple wildcard nodes exist, we follow a fixed order that prioritizes those with the largest distance from the output and the left child of a gate over the right one. For multi-output cases, we generate the circuit for each output separately, and combine them together via node merging which will be discussed in the next section.

For the selection of logic gates (vocabulary list) in the sequential representation, we note that the combination of AND and NOT gates can express all possible truth tables of Boolean functions (which is termed "functional completeness"), and is also commonly adopted in practical circuit representation [2]. Therefore, we adopted this setting, with an alteration that we merged the NOT gate with the AND gate and primary inputs. Instead of assigning the NOT gate an individual token, each primary inputs and the AND gate has two versions: the original ones ($x_1, \ldots, x_N, \wedge$) and the inverse ones ($\overline{x_1}, \ldots, \overline{x_N}, \overline{\wedge}$), so the vocabulary list contains $2N + 2$ tokens in total[3]. This allows us to significantly shorten the sequence with a moderate increase of vocabulary size.

An example of our proposed representation and cutoff properties are shown in Figure 3. We leave the proof of Characteristic 3.1, 3.2, 3.3 and 3.4 in the appendix.

3.3 From Trees to Directed Acyclic Graphs

In the last section, we proposed a sequential representation of circuits based on recursive replacement of wildcard nodes in the top-down manner. Such an approach implicitly assumes that a logic gate

[3]This does not include special tokens such as [EOS] and [PAD] in Transformer models.

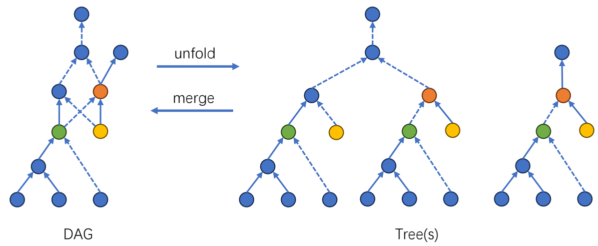


Figure 4: Transition between a DAG and one or more trees. The shown DAG is an abstraction of Figure 1c in which circles represent AND gates, primary inputs and outputs, solid arrows represent wires from outputs to inputs, and dashed arrows represent wires with a NOT gate between the input and the output.

would always have one fan-out[4], restricting the generated circuits to be highly hierarchical with tree structures. However, multi-fanout gates do commonly exist in real-world logic circuits, which shape circuits as directed acyclic graphs (DAGs).

In this section, we show how we extend our method to generate DAG circuits. We notice that a DAG can be "unfolded" to one or more trees once we duplicate every node with outdegree larger than one, so that every node has at most one outgoing edge. For example, the orange node in the left DAG of Figure 4 is duplicated into two individual nodes, where its two outgoing edges are assigned respectively. Reversely, one or more trees can also be transformed to a DAG by merging nodes with structural equivalence. For circuits, such a bidirectional transition will not change the Boolean function it represents. Therefore, we generate a DAG circuit by firstly generating its unfolded tree representation, and then merging equivalent nodes in the generated tree representation. In logic circuit design, different nodes can be not only structurally equivalent but also functionally equivalent [26], which means that their outputs represent the same Boolean functionality. Functionally equivalent nodes can thus be merged as a single node even if they have different underlying structures. Our approach mainly leverages the functional equivalence.

3.4 Neural Encoding of Circuits and Circuit Transformer

While we can deserialize our proposed sequential representation to a DAG circuit via node merging, we can also serialize a given DAG circuit to our proposed sequential representation via a depth-first traversal with node duplication. Given a DAG circuit, we start a traversal from each of its primary outputs, and visit each connected gate in a depth-first, recursive manner. Backtracking occurs when a primary input is reached. Importantly, such a traversal is memory-less, i.e., visited nodes will not be labelled during the traversal, thus a node will appear multiple times in the trajectory if its fan-out is larger than one, corresponding to the node duplication in the last section. When the process is finished, the traversal trajectory $s_1, \ldots, s_n$ is the sequential representation of the unfolded tree version of the original DAG circuit. Note that such an unfolding process may lead to long sequences, especially for nodes with large number of fan-outs. A more compact representation is leaved as future work.

For Transformer models to process the sequential representation, it is important to provide an efficient positional encoding for each node to indicate its position in the circuit. In this work, we utilize the path from the primary output to a given node to indicate the node's position. To achieve this, we follow [33] that encodes the path as a stack of one-hot encodings ("10" for the first input and "01" for the second input). More details are leaved in the appendix.

With all the circuit encoding and generation techniques introduced above, we propose Circuit Transformer, an end-to-end Transformer model that generates a new and functionally equivalent circuit of the input one. The Transformer uses an encoder-decoder architecture, and the original circuit is serialized to our proposed sequential representation, acting as the input of the Transformer encoder. The Transformer's decoding process cooperates with the backtrack programming framework in Algorithm 1 with our proposed cutoff properties in Section 3.2. Given Characteristic 3.3, the backtrack process in line 11-14 will not be actually executed, so S_t in line 4 of Algorithm 1 reduces to a masking layer at the end of the Transformer decoder, filtering invalid tokens by assigning probability zero to them. Finally, node merging proposed in Section 3.3 is applied to the decoded sequence to transform the unfolded tree representation to a DAG circuit. The pipeline is shown in Figure 2.

[4]The fan-out of a gate is the number of inputs driven by the output of the gate.

3.5 Equivalent Circuit Generation as a Markov decision process

An important application of equivalent circuit generation is to optimize circuits with respect to certain objectives. For example, in semiconductor industry, it is of vital importance to reduce the size of a given circuit measured by the number of logic gates, while the specification of the circuit (i.e., the Boolean function it represents) keeps equivalent. Under our proposed sequential representation, it can be achieved by attaching an immediate reward function $R(s_1, \ldots, s_t, s)$ to the generation of token s at step t, so that the sum of the reward function throughout the generation reflects the objective. In this way, the generation process can be regarded as a deterministic Markov decision process, in which the state at step t is the generated tokens $s_1, \ldots, s_t$, the set of actions available from the state is $S_t = \{s \in D | F(s_1, \ldots, s_t, s; f) \text{ holds}\}$, the immediate reward is $R(s_1, \ldots, s_t, s)$, and the next state is $s_1, \ldots, s_t, s$ with probability 1. The process terminates once $s_1, \ldots, s_t$ represents a unique circuit with all wildcard nodes replaced. Such a formulation owns two key advantages. First, the feasibility of the generated circuit is guaranteed once the process terminates. No effort is required to penalize infeasible cases via crafting the reward function. Second, the size of the available action set is at most $2N + 2$, in which N, the number of inputs, is usually moderately small in practice. Other circuit representations typically assign each logic gate a unique ID to describe their adjacency, requiring the size of available actions to be proportional to the number of gates, which is usually significantly larger than N.

For the circuit size minimization problem in Equation 3, the immediate reward function can be defined as

$$R(s_1, \ldots, s_t, s) = \Delta + \begin{cases} -1, & s = \wedge \text{ or } s = \overline{\wedge} \\ 0, & \text{otherwise} \end{cases} \tag{9}$$

in which Δ reflects the refinement due to equivalent node merging. Given a depth-first replacement order of wildcard nodes in Section 3.2, the node merging process in Section 3.3 can be done simultaneously with the generation process, whose detail is leaved in the appendix.

4 Experiments

In this section, we supervisedly train a Circuit Transformer to solve the circuit size minimization problem in Equation 3, generating equivalent yet more compact forms of input circuits, and conduct extensive experiments on both synthetic and real-world datasets to evaluate its feasibility and optimality.

The details of the Circuit Transformer model are as follows. We employed an encoder-decoder architecture following [41], each with 12 attention layers. The embedding width and the size of feedforward layer are set as 512 and 2048 respectively, leading to 88,225,800 total parameters. The vocabulary size is 20 (8 inputs and the AND gate, with their inverse, plus [EOS] and [PAD]). Batch size is set to be 128. The maximum length of the input and output sequence is set to be 200. To evaluate the effectiveness of tree positional encoding (TPE) in Section 3.4, we trained Circuit Transformers with and without TPE. The maximal depth of tree positional embeddings is set to be 32. The implementation is based on [49].

We also trained two baseline Transformer models with exactly the same experimental settings, except employing different sequential representation of circuits as follows:

- Boolean Chain [15]: a representation that is extensively applied in SAT-based optimization techniques. A chain is initialized by all the primary inputs of the circuit, and each gate is represented by two prior indices in the chain, indicating the source of its two inputs.
- AIGER [2]: a popular representation of logic circuits with AND and NOT gates. We follow the tokenization setting in [31], representing an AND gate by three tokens followed by a special new line token.

To train and evaluate the Circuit Transformer model, we build a large dataset containing 15 million randomly generated 8-input, 2-output circuits. The supervised signals (i.e., the equivalent circuits that are optimized in size) are generated by the Resyn2 command in ABC [3], a representative optimization flow for circuit size minimization. The detail of random circuit generation is leaved in the appendix. 89% of the data is for training, 1% is for validation and 10% is reserved for testing. All the Transformer models are trained on the training set sufficiently for 5 epochs.

Methods	Random circuits		IWLS FFWs	
	Unsuccessful cases	Average circuit size	Unsuccessful cases	Average circuit size
Boolean Chain	5.07% (5.07%)	15.25	11.36% (11.26%)	17.24
Boolean Chain (beam size = 16)	2.16% (2.16%)	14.89	6.34% (6.29%)	17.15
Boolean Chain (beam size = 128)	1.91% (1.91%)	14.87	5.97% (5.94%)	17.15
AIGER	4.32% (4.32%)	15.14	8.35% (7.77%)	17.19
AIGER (beam size = 16)	1.85% (1.85%)	14.87	4.62% (4.37%)	17.12
AIGER (beam size = 128)	1.71% (1.71%)	14.86	4.24% (3.99%)	17.12
Circuit Transformer w/o TPE	2.14% (0%)	15.02	6.63% (0%)	17.33
Circuit Transformer	1.14% (0%)	14.79	4.76% (0%)	17.17
Circuit Transformer ($K = 10$)	0.20% (0%)	14.02	2.83% (0%)	16.92
Circuit Transformer ($K = 100$)	**0.17%** (0%)	**13.73**	**2.63%** (0%)	**16.73**
Resyn2 (ground truth for training)	/	14.56	/	16.82

Table 2: Results on 10,240 randomly generated circuits, and 10,240 fanout-free windows randomly sampled from the IWLS 2023 benchmark. For unsuccessful cases, the percentage in the bracket corresponds to failures due to equivalence constraint violation. All results of Circuit Transformers show zero violation of equivalence constraints. K denotes the total number of playouts in Monte-Carlo tree search. All the models are supervisedly trained on the Resyn2 optimized circuits.

We employ both a synthetic dataset and a real EDA benchmarks to evaluate the performance of the models:

- Random circuits: 10,240 circuits are randomly sampled from the test set of the aforementioned randomly generated dataset.
- IWLS FFWs: we transform the IWLS 2023 benchmark [24] into circuits represented by AND and NOT gates by the script suggested in [25], and extract 1.5 million 8-input, 2-output fanout-free windows (FFWs) [54]. Then we randomly sample 10,240 circuits from the extracted FFWs.

The latter is of significance in practice, as sub-circuit optimization acts as the core technique of large circuit optimization.

To enhance the performance of the Transformer models in comparison, two heuristics search techniques are applied. Beam search is applied for Transformer models on Boolean chain and AIGER represented circuits. Monte-Carlo tree search is applied for Circuit Transformer to evaluate our proposed MDP formulation in Section 3.5. The detail is leaved in the appendix.

The results are presented in Table 2. On both synthetic and real datasets, the Circuit Transformer surpasses two other Transformer models in terms of feasibility (measured by the percentage of unsuccessful cases) and optimality (measured by the average circuit size). The two baseline models generate unsuccessful circuits for various reasons, including equivalence constraint violations, cycles in circuits, or incomplete specifications, with the most common issue being that the generated circuit is complete and valid but not strictly equivalent to the original. In contrast, the Circuit Transformer's exact precision is empirically shown by zero violation of complex equivalence constraints. The only reason for unsuccessful cases is that wildcard nodes are not fully replaced within the given maximum sequence length of 200. Regarding heuristic search enhancement, while beam search significantly improved feasibility, consistent with findings in [31], the issue of non-equivalence remained prevalent. Conversely, Monte-Carlo tree search in the Circuit Transformer not only substantially reduced unsuccessful cases but also significantly improved the average circuit size, sometimes producing circuits more compact than the ground truth with a moderate number of playouts.

5 Conclusion

In this work, we make an important advancement towards achieving precise generative AI for logic tasks, demonstrating that complex hard-constraint satisfaction is attainable for next-token prediction models when a proper formulation of the constrained problem is established. Inspired by the backtrack programming framework, we introduce a novel approach to the fundamental problem of equivalent circuit generation, enabling next-token prediction models to generate new logic circuits while strictly adhering to complex equivalence constraints. This methodology has the potential to be extended to other fundamental constrained problems, making it a promising area for further research.

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A Appendix / supplemental material

A.1 Detail of Backtrack Programming Framework

The basic backtrack algorithm is as follows, extracted from [16]:

Given domain D and properties $F(s_1, \dots, s_t)$, this algorithm visites all sequence $s_1, s_2, \dots, s_n$ that satisfy $F(s_1, \dots, s_n)$:

Step 1 [Initialize] Set $t \leftarrow 1$, and initialize the data structures needed later.
Step 2 [Enter level t] (Now $F(s_1, \dots, s_{t-1})$ holds.) If $t > n$, visit $s_1, \dots, s_n$ and go to Step 5, Otherwise set $s_t \leftarrow \min D$, the smallest element of D.
Step 3 [Try s_t] If $F(s_1, \dots, s_t)$ holds, update the data structures to facilitate testing $F(s_1, \dots, s_t, s_{t+1})$, set $t \leftarrow t + 1$, and go to Step 2.
Step 4 [Try again] If $s_t \neq \max D$, set s_t to the next larger element of D and return to Step 3.
Step 5 [Backtrack] Set $t \leftarrow t - 1$. If $t > 0$, downdate the data structures by undoing the changes recently made in Step 3, and return to Step 4. (Otherwise stop.)

The following example shows how cutoff properties can be invented for a specific problem to be solved by backtrack programming. To generate all permutations $s_1, \dots, s_n$ of $\{1, \dots, n\}$ in which all numbers should appear exactly once, we can set $s_i \in \{1, \dots, n\}, i = 1, \dots, n$, and the cutoff property $F(s_1, \dots, s_t)$ holds at step t if and only if $s_i \neq s_j, \forall 1 \leq i < j \leq t$. In such a way, Characteristic 3.1 is obvious, and Characteristic 3.2 also holds, as we only need to test whether $s_i \neq s_t$ holds for all $1 \leq i < t$ given $F(s_1, \dots, s_{t-1})$ holds.

We refer to Section 7.2.2 of [16] for more details about backtrack programming.

A.2 Proof of Characteristics

In this section, we demonstrate that our proposed sequential representation owns Characteristic 3.1, 3.2, 3.3 and 3.4.

Characteristic 3.1: When $F(s_1, \dots, s_{t+1}; f)$ is true, the transition from $s_1, \dots, s_{t+1}$ to $s_1, \dots, s_t$ corresponds to reversely replacing a specific node s_{t+1} with a wildcard node. such a replacement will never break the feasibility, because (1) a wildcard node only represents feasible circuits; (2) the wildcard node at least have a feasible choice to be set as s_{t+1} as $s_1, \dots, s_{t+1}$ is feasible.

Characteristic 3.2: During the generation from step 1 to step $t - 1$, a caching mechanism can be employed to cache the truth table of the constructed nodes. Therefore, when $F(s_1, \dots, s_{t-1}; f)$ holds and $F(s_1, \dots, s_{t-1}, s_t; f)$ needs to be evaluate, we simply traverse the generated circuit in a bottom-up manner, from the current wildcard node to be replaced to the root, to evaluate $g^{(t)(\boldsymbol{x})}$ for all $x \in \{0, 1\}^N$ with time complexity of $O(2^N \cdot d)$ in which d is the depth of the node. More details about the caching mechanism can be found in `check_conflict_batch_new` in `utils.py`.

Algorithm 2 Circuit generation with immediate equivalent node merging

Input: The Boolean function f that the generated circuit should be equivalent to. Next token prediction model $P(s_t|s_1,\ldots,s_{t-1})$.
Output: A feasible circuit g satisfying $g \in C(f)$.

Initialize $path$ as an empty stack of gates, POs as an empty list.
Initialize $G = \emptyset$ as a set of non-isomorphic gates
for $t = 1, 2, 3, \ldots$ **do**
  Compute a probability distribution of $s_t \in D$ by the next token prediction model

$$p_t \leftarrow P(s_t|s_1,\ldots,s_{t-1})$$

  Set $S_t \leftarrow \{s \in D | F(s_1,\ldots,s_{t-1},s;f) \text{ holds}\}$ ▷ $S_t \neq \emptyset$ is guaranteed by Characteristic 3.3
  $s_t \leftarrow \arg\max_{s \in S_t} p_t(s)$
  Initialize $s_t.input1 \leftarrow U, s_t.input2 \leftarrow U$ if s_t is a gate.
  if $path$ is empty **then** ▷ the output of s_t is the primary output of the circuit
    Append s_t to POs and push s_t to $path$
  else ▷ s_t should be the input of the last gate in $path$
    $s \leftarrow path.peek()$ ▷ get the last gate added to $path$
    if $s.input1 = U$ **then** $s.input1 \leftarrow s_t$ **else** $s.input2 \leftarrow s_t$ ▷ replace a wildcard node in s_t to s
    if s_t is a gate **then**
      $path.push(s_t)$
    else ▷ s_t is an input node in $x_1, \overline{x_1}, \ldots, x_N, \overline{x_N}$. Pop fully constructed gates from $path$
      while $s.input1 \neq U$ **and** $s.input2 \neq U$ **do**
        if $s \in G$ **then** ▷ Compute the truth table of s to check functional equivalence
          Update $path$ and POs to replace s with the functional equivalent one in G
        else
          Add s to G
        end if
        $s \leftarrow path.pop()$
      end while
    end if
  end if
end for
Return the circuit with POs as POs

Characteristic 3.3: Note that the AND gate $\wedge$ and the NAND gate $\overline{\wedge}$ is always in S_t in our sequential representation, as replacing a wildcard node to an AND or NAND gate with two wildcard nodes will never break the feasibility.

Characteristic 3.4: For all $g \in C(f)$, the sequence $s_1, \ldots, s_n$ that represents g is demonstrated in Section 3.4.

A.3 Demonstration of The Tree Positional Encoding

For example, in Figure 2, the position of the second node in the sequence, i.e., the uppermost AND gate connecting x_1 and x_2, can be represented as $e_2 = [10]$ (this gate's output is the first input of the rightmost AND gate, so "10" is pushed in the encoding stack of the rightmost AND gate, which is empty), and the position of the fourth node x_2 in the sequence can be represented as $e_4 = [01; e_2] = [0110]$ (push "01" in e_2 as x_2 is the second node's second input) and $e_6 = [10; e_5] = [1001]$ when x_2 is secondly visited as the fifth node's first input.

For circuits with multiple primary outputs ($M > 1$), we initialize the encoding stack of each primary output with a unique one-hot encoding, as if there is a virtual root node of M children, and each primary output corresponds to one of the children.

A.4 Immediate Equivalent Node Merging and Functional Equivalence Checking

With a depth-first replacement order, we can follow Algorithm 2 to merge equivalent nodes during the generation process. For functional equivalence checking of two nodes p and q, we check whether $p(\boldsymbol{x}) = q(\boldsymbol{x}), \forall \boldsymbol{x} \in \{0,1\}^N$ by iterating all $\boldsymbol{x}$. If there is an $\boldsymbol{x}$ such that $p(\boldsymbol{x}) \neq q(\boldsymbol{x})$, then p and q are not functionally equivalent.

Algorithm 3 Circuit Generation with Monte-Carlo Tree Search

Input: The Boolean function f that the generated circuit should be equivalent to. Next token prediction model $P(s_t|s_1, \ldots, s_{t-1})$. Immediate reward function $R(s_1, \ldots, s_t)$. Number of playouts K.
Output: A feasible circuit g satisfying $g \in C(f)$.
procedure PUCT(an MCTS node x)
  for a in x's all child nodes **do**
    $s_a \leftarrow \frac{a.\text{total\_value}}{a.\text{visited}} + a.\text{prob}\sqrt{\frac{x.\text{visited}}{1+a.\text{visited}}}$
  end for
  Return $\arg\max_a s_a$
end procedure
procedure MCTS(P, R, K) ▷ See [34] for details
  Create a root MCTS node r
  for $i = 1, 2, \ldots, K$ **do**
    (Selection) Starting from r, iteratively selects a child node via PUCT algorithm until reaching a leaf node l.
    (Expansion) Evaluate l via $P(s_t|s_1, \ldots, s_{t-1})$ (i.e., create all child nodes a for l, and assign a.prob for each child via $P(s_t|s_1, \ldots, s_{t-1})$), and select a valid child node (cutoff properties F holds) via PUCT.
    (Simulation) Run the generation process from the selected node via Algorithm 2 until a complete circuit is generated or the maximum #(iter) is reached, and get the cumulative reward v
    (Backpropagation) Update the "visited" and "total_value" attributes of the MCTS nodes from p to r in a backward pass with v.
  end for
  Return The path from r to the leaf node with maximal "total_value" attributes.
end procedure
Get optimized sequence $s_1, \ldots, s_t$ from MCTS(P, R, K).
Given $s_1, \ldots, s_t$, continue the generation process in Algorithm 2 and return the generated circuit.

Algorithm 4 Random generation of a k-input, l-output circuit

Input: Number of input k, number of output l, number of steps T.
Output: A randomly generated circuit with k inputs and l outputs.
$C \leftarrow [I_0, I_1, \ldots, I_{k-1}]$
for $i = 1, 2, \ldots, M_{\text{step}}$ **do**
  Create an AND node s_i
  Randomly sample two nodes $c_0, c_1 \in C$ without replacement
  Set the first input of s_i as c_0 or $\overline{c_0}$ randomly
  Set the second input of s_i as c_1 or $\overline{c_1}$ randomly
  Append s_i to the end of C
end for
Return the circuit with $I_0, I_1, \ldots, I_{k-1}$ as primary inputs and $a_{T-l+1}, a_{M-l+2}, \ldots, a_T$ as primary outputs.

A.5 Monte-Carlo Tree Search for Circuit Size Minimization

The search process is sketched in Algorithm 3.

A.6 Dataset Generation

The process to generate a random circuit is shown in Algorithm 4. We restrict that the length of the encoded sequence for each circuit should fit all the three sequential representations with a maximal length of 200, and all the 8 inputs should appear in the circuit. Each circuit has a unique structure, which is realized by a canonicalization technique [4].

A.7 Experiments Compute Resources

All the experiments are conducted on a workstation with the following specification:

- CPU: AMD Ryzen™ 9 7950X Desktop Processor (16 cores, 32 threads)
- Memory: 192GB (48GB $\times$ 4) DDR5 5200MHz
- GPU: NVIDIA GeForce RTX 4090 $\times$ 2

Each Transformer model in the experiments is trained on a single GPU with 75 hours.

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